

IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An integrated circuit (IC) comprising:
at least one circuit element;
a node coupled to the at least one circuit element;
at least one non-floating terminal on a surface of the integrated circuit (IC) to mount to a corresponding pad on a substrate, wherein the at least one non-floating terminal comprises a first solder bump and a first conductor;
at least one floating terminal on the surface of the integrated circuit (IC) to mount to a corresponding pad on the substrate, wherein the at least one floating terminal comprises a second solder bump, a second conductor, and at least one dielectric layer physically separating and in physical contact with the second solder bump and the second conductor; and
at least one coupling element to couple any combination of the at least one floating terminal and the at least one non-floating terminal to the node.
2. (Currently Amended) The integrated circuit (IC) recited in claim 1 wherein the node is selected from the group consisting of power nodes, ground nodes, and input/output nodes.
3. (Currently Amended) The integrated circuit (IC) recited in claim 1 wherein the second solder bump, second conductor, and at least one dielectric layer of the at least one floating terminal form at least one floating terminal comprises a capacitive element.
4. (Currently Amended) The integrated circuit (IC) recited in claim 3 wherein the first conductor and the second conductor capacitive element comprises a connector element, at least one dielectric layer, and a conductor that can be selectively coupled to the node.

5. (Currently Amended) The integrated circuit (IC) recited in claim 4 wherein the substrate pad is selected from the group consisting of a power terminal, a ground terminal, and an input/output terminal ~~connector element comprises a solder bump~~.
6. (Currently Amended) The integrated circuit (IC) recited in claim 1 wherein the at least one coupling element comprises selector logic coupled to the at least one floating terminal, to the at least one non-floating terminal, and to the node, and comprising at least one control input, at least one logic element coupled to the at least one control input, and at least one output to couple any combination of the first and second conductors to the node.
7. (Currently Amended) An integrated circuit (IC) comprising:
a plurality of circuit elements;
a plurality of nodes coupled to the plurality of circuit elements;
a plurality of non-floating terminals on a surface of the integrated circuit (IC);
at least one floating terminal on the surface of the integrated circuit (IC); and
selector logic coupled to the terminals and to the plurality of nodes to couple any combination of the at least one floating terminal and one of the plurality of non-floating terminals to one of the plurality of nodes.
8. (Currently Amended) The integrated circuit (IC) recited in claim 7 wherein the one node is selected from the group consisting of power nodes, ground nodes, and input/output nodes.
9. (Currently Amended) The integrated circuit (IC) recited in claim 7 wherein the at least one floating terminal comprises a capacitive element.
10. (Currently Amended) The integrated circuit (IC) recited in claim 9 wherein the capacitive element comprises a connector element, at least one dielectric layer, and a conductor that can be selectively coupled to the one node.

11. (Currently Amended) The integrated circuit (IC) recited in claim 10 wherein the connector element comprises a solder bump.
12. (Currently Amended) The integrated circuit (IC) recited in claim 7 wherein the selector logic comprises at least one control input and further comprises at least one output to selectively couple any combination of the at least one floating terminal and one of the plurality of non-floating terminals to the one node.
13. (Currently Amended) An electronic assembly comprising:
an integrated circuit having (IC) comprising:
at least one circuit element;
a node coupled to the at least one circuit element;
at least one floating terminal on the surface of the integrated circuit (IC) to mount to a corresponding pad on a substrate, wherein the at least one floating terminal comprises a solder bump, a conductor, and at least one dielectric layer physically separating and in physical contact with the solder bump and the conductor; and
at least one coupling element to switchably couple the at least one floating terminal to the node; and
an integrated circuit (IC) package substrate comprising a plurality of pads and internal circuit paths, including at least one pad and at least one internal circuit path to couple to the at least one floating terminal.
14. (Currently Amended) The electronic assembly recited in claim 13 wherein the solder bump, conductor, and at least one dielectric layer form a capacitive element at least one floating terminal comprises a capacitive element, and wherein the capacitive element comprises a connector element coupled to the at least one pad, at least one dielectric layer, and a conductor to be switchably coupled to the node.

15. (Currently Amended) The electronic assembly recited in claim 13 wherein the at least one coupling element comprises selector logic coupled to the at least one floating terminal and to the node, and comprising at least one control input, at least one logic element coupled to the at least one control input, and at least one output to couple the conductor of the at least one floating terminal to the node.

16. (Currently Amended) A method of testing an integrated circuit (IC) comprising a plurality of circuit elements and a plurality of terminals including at least one floating terminal, the method comprising:

testing the integrated circuit (IC);

identifying at least one circuit element that is not optimally functioning; and

coupling the at least one floating terminal to the at least one circuit element.

17. (Currently Amended) The method recited in claim 16 wherein the integrated circuit (IC) is selected from the group consisting of a microprocessor, a microcontroller, a graphics processor, a digital signal processor, an application-specific integrated circuit, a memory circuit, a communications circuit, an artificial intelligence circuit, a neural network, a logic circuit, a computational circuit, a processing circuit, a sensing circuit, a transducer circuit, a power circuit, an amplifying circuit, a data conversion circuit, a data transmission circuit, a data receiving circuit, a custom circuit, and a control circuit.

18. (Currently Amended) The method recited in claim 16 wherein the integrated circuit (IC) comprises a plurality of floating terminals and selector logic coupled to the plurality of floating terminals, and wherein the method further comprises:

providing at least one control signal to the selector logic; and

the selector logic coupling at least one floating terminal to the at least one circuit element.

19. (Currently Amended) The method recited in claim 18 wherein the integrated circuit (IC) further comprises a plurality of non-floating terminals, and wherein the method further comprises:

- providing at least one control signal to the selector logic; and
- the selector logic coupling at least one floating terminal and at least one non-floating terminal to the at least one circuit element.

20. (Currently Amended) The method recited in claim 18 wherein the integrated circuit (IC) further comprises a plurality of non-floating terminals, and wherein the method further comprises:

- providing at least one control signal to the selector logic; and
- the selector logic coupling either a floating terminal or a non-floating terminal, but not both, to the at least one circuit element.

21. (Currently Amended) The method recited in claim 16 wherein the integrated circuit (IC) further comprises a plurality of floating and non-floating terminals, and selector logic coupled to the floating and non-floating terminals, and wherein the method further comprises:

- providing at least one control signal to the selector logic; and
- the selector logic coupling any combination of floating and non-floating terminals to the at least one circuit element.

22. (Currently Amended) The method recited in claim 16 wherein the integrated circuit (IC) comprises at least one floating power terminal, at least one non-floating power terminal, at least one floating ground terminal, at least one non-floating ground terminal, the terminals being coupled to the at least one circuit element, and the integrated circuit (IC) further comprising selector logic coupled to the terminals, and wherein the method further comprises:

- providing at least one control signal to the selector logic; and
- the selector logic coupling any combination of floating and non-floating terminals to the at least one circuit element.

23. (Currently Amended) The method recited in claim 22 wherein the integrated circuit (IC) further comprises at least one floating input/output (I/O) terminal, and at least one non-floating input/output (I/O) terminal, the at least one floating input/output (I/O) terminal and the at least one non-floating input/output (I/O) terminal being coupled to the at least one circuit element and to the selector logic, and wherein the method further comprises:

providing at least one control signal to the selector logic; and
the selector logic coupling any combination of floating and non-floating terminals to the at least one circuit element.

24. (Currently Amended) A method of fabricating an integrated circuit (IC) comprising a circuit element and a plurality of non-floating terminals coupled to the circuit element, the method comprising:

determining a subset of the plurality of non-floating terminals whose operational characteristics may require adjustment when the integrated circuit (IC) is operating; and
providing a floating terminal for each of the subset of non-floating terminals.

25. (Currently Amended) The method recited in claim 24 wherein the operational characteristics comprise resistive-capacitive (RC) characteristics.

26. (Currently Amended) The method recited in claim 24 wherein at least one of the subset of non-floating terminals is selected from the group consisting of a power terminal, a ground terminal, and an input/output terminal.

27. (Currently Amended) The method recited in claim 24 and further comprising:
providing an integrated circuit (IC) package substrate comprising a plurality of pads and internal circuit paths, including at least one pad and at least one internal circuit path to couple to each of the floating terminals; and
mounting the integrated circuit (IC) on the integrated circuit (IC) package substrate.

PRELIMINARY AMENDMENT

Serial Number: Unknown

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Assignee: Intel Corporation

Page 8

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28. (Original) The integrated circuit recited in claim 1 wherein the at least one circuit element is selected from the group consisting of a digital logic circuit, an analog circuit, a power circuit, a sense circuit, an amplifier circuit, and a radio circuit.

29. (Original) The integrated circuit recited in claim 1 wherein the at least one circuit element comprises an inverter circuit.